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Yield Improvement for a new MCM/SiP IC using TRIZ Processes

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Abstract

Semiconductor packaging technology is advanced and sophisticated for high integration. The MCM and SiP is a modern technology used in IC packaging. It consists of passive tens components, multi chips and more than a hundred wires on the substrate. Low yield often happens in assembling process when introducing a new product or process and it is difficult to find out the root cause in such a sophisticated and highly integrated MCM IC. In this project, low yield problem for a new MCM IC assembling process was analyzed and solved by using TRIZ systematic procedures. The Function Analysis (FA) diagram described the relationship of the components and devices in the MCM package. In the FA, we used FA for device to analyze the total system of MCM and FA for process to analyze the MCM assembling process. CECA was used to figure out the negative factors including target factors and key factors. The CECCA was used to locate contradictions in order to get a clearer picture of the root cause problem of the MCM assembling system. Finally we used FA-solution directive to solve the problem of the process and improve the yield. At the end, the yield problem was resolved from almost 0% to 99% saving millions of NT Dollars for the new product introduction. This project presents a systematic procedure to solve the complex system.

Key words: MCM, SiP, substrate, yield, TRIZ, FA, CECA, CECCA.

1. Introduction

In the advanced semiconductor industry, complex package is used massively in a variety of ICs. In the complex MCM packaging process, low yield happens in assembling process. We use a series of systematic methodology to analyze the problem and find out the root-cause efficiently.

This paper presents the Function Analysis (FA) diagram, which describes the relationship of the components and devices in the MCM package. In the FA, we use FA for device to analyze the total system of MCM and to analyze the MCM assembling process. We used CECA to figure out the negative factors including target factors and key factors. The CECCA were used to locate contradictions in order to get a clearer picture of the root cause problem of the MCM assembling system. Finally we used FA-solution directive to solve the problem of the process and improve the yield.

At the end, the yield problem was resolved from almost 0% to 99% saving millions of NT Dollars for the new product introduction.

2. Package Assembling Process

2.1 Main Functions and Constraints of the System

The assembling system discussed in this research is a Multichip Module IC assembling for a wireless Audio Application. There are 5 chips (ICs) built in a single package. The assembling processing includes passive components SMT, die bonding, wire bonding, and molding. The yield of wafers (chips) and SMT process quality affect the total yield of assembling. And the ICs cannot be 100% good in real world. Therefore, the assembling yield could be 99% x99% x99%x 99%x 99%=95%. Yet that is an acceptable yield in the RF products.

However, if there are some mistakes in processes, the yield will be very low. Since the cost of wafers is very high, we need to find a good way to increase the assembling yield. It is a very important way to make profit and fulfill customer's delivery schedule.

2.2 Purpose of the Systematic System

The processes of assembling include PCB fabrication, SMD on the PCB substrate, die /wire bonding, molding, baking, laser marking and singulation (chip sawing). After the assembling processes, we need to do final test to screen out bad products. In this study, a 2.4 GHz audio MCM IC was assembling and we will use TRIZ to improve low yield problems.

The IC is a high value product which contains 5 chips and 46 passive components with 146 Au-wires. So, it is very important to maintain high assembling yield. However, many elements, such as Chip yield, SMT yield, die bond, wire bond, and molding quality, may affect the assembling yield. Our target assembling yield is 95%. There are 3 CMOS chips and 2 GaAs chips in this SiP. The CMOS wafers are all probed, but the GaAs wafers are not probed because they are for high frequency RF application.

The probing process is difficult and expensive which uses high frequency RF equipment and testing system. There are 46 passive components on the BT substrate. The SMT process will cause loss as well. Die bond and wire bond will fail in certain degree. Thus, it generates yield loss after processing. If the yield can be 95+%, the assembling process will be recognized as a proper process. The yield loss of assembling comes from a set of workings such as: SMT, die bond/wire bond, molding, Laser Marking and IC molding. If we can add some kind of inspection steps to the process, it will guarantee high yield (optimum 98 %+) in the process.

During the Chinese New Year holidays in 2013, our company lost 15000 pcs of SiP IC at an yield of 0%. After checking the test results, we found the problem was chip failure. We checked the surface of the chips, using Microscope under 2000 X. We found there were some pouched holes on the chips. How did it happen? Who did this? The priority here is to find out what caused the holes on the chips and try to retrieve a yield of 95% because customers are waiting for the IC to delivery of our final product.

Table 1. MCM assembling flow

Flow	Description
Substrate	Substrate can be laminated poly-glass or ceramic (LTCC).
Solder past	Solder paste contains 95% Tin and 5% antimony alloy with 0.5% flux.
SMT passive com	Passive components-Resistors, Capacitors and Inductors. Their compositions are ceramic powder with metal terminals.
Reflow	Reflow system using electro-thermal paste dissolves into Tin, passive components are attached to the base plate of metal welding points.
Baking	Baking removed the water within the electric baseboard.
Die bond	Die bond is that an IC chip with silver adhesive bonded on the die paddle. The silver epoxy is 99% silver powder and 1% Binder.
Curing	Baking: the silver adhesive is curried.
Plasma Clean	Plasma cleaning: using argon gas-free electronics, impacting the chip surface achieving the clean results.
Wire Bond	Wire bond: use of ultrasound energy and heating to weld gold wire on chip and substrate.
Vision Checking	According to customer's requirement and specification entitled inspection of product quality.
Molding	Molding: black plastic coating on the chip to reaches proofing and protective effect, Black gum's main ingredients are ceramic powder and charcoal powder to protect the know how in the IC.
Baking	Baking: Using the oven to cure the molding compound material to protect IC.
Laser Marking	Laser marking (Print): with white ink or laser marking to indicate product number and manufacture date on the product.
Singulation	Singulation: saw the substrate into small pcs using cutter and tools.
Testing	Testing: before tape and reel, we need to test based specs.
Tape and Reel	Tape and reel (Packing): pack the single unit piece by piece using plastic tape.
Dry Pack	Vacuum and Dry packing with MSL indicator
Delivering	Shipping: finished products through inspection, packing and transport.

2.3 Constraints

In the system, we need to face two constraints, namely business constraint and technical constraint, and put them into our consideration. The key processing is die bonding.

The business constraints are:
(1) The cost for RF wafer probe is high.
(2) It needs more human power if we add steps to the process to double check.
(3) In a mature IC assembling factory, the final yield is expected to be higher than 95%.

The technical constraints are:
(1) The subcontractor is the one who is responsible for the process in packaging house.

The IC designer has no right to check the assembling processing in the factory.
(2) After molding, there is not a chance to fix the IC because the parts and dies are covered by the molding material.

The two constraints were brought up in the following analysis.

3. Analysis and Procedures

The procedure has 4 steps: defining, selecting tool, generating solution and evaluating. The defining stage is to analyze the problem (case) and then select the right tool to solve the problem.

In the current study, we used the systematic procedures from TRIZ tools which systematically check all the affected parameters step by step.

- The tools are:
- Function Analysis
- Interaction Matrix
- FA diagram
- All of function disadvantages
- Cause Effect and contradiction Chain Analysis
- Sub fields Analysis
- Patent and Web Search
- FOS

In the case presented in the paper, the process is a complete MCM/ SiP IC assembling, which includes PCB SMT, plasma clean, die bonding, curing, wire bonding, molding, aser marking, and sawing. After detailed analysis we found the key problems lied in die bonding. We will present and analyze the key part of the process: die bonding in the following sections.

3.1 Function Analysis (FA) for Die Bonding

FA is the abbreviation of function analysis. It separates the components in order to figure out the relationships among components. Which of them are targets? Which of them are tools? Which one of them is the main function? Which one of them is the auxiliary function? Which are positive and negative functions? Those harmful, excess, and insufficient functions are all categorized as negative functions. From negative functions and other related functions, we can find contradictions and easily focus on the problems.

Table 2. Function Analysis for die bonding

System: die bonding process			
System Components		**Super System Components**	
Die Collet		PCB with SMD	
Preciser		Conductive Epoxy	
Die Bonding Nozzle		Die	

In the Super System, there are components such as PCB with SMD, conductive Epoxy, and die. The System components are Die Collet, Preciser, and die bonding nozzle.

- Interaction Matrix of bonding processing

Through FA, we found out the interactions between components. Based on the FA, we built an interaction matrix of die bonding processing. It shows the interactions between components and their way of interacting.

Table 3. The interaction matrix of bonding processing

System: Yield Improvement for MCM IC

+: interact
-: No relation

From-To	Die Collet	Preciser	Die Bonding Nozzle	PCB with SMD	Conductive Epoxy	Die
Die Collet	X				+	+
Preciser		X				+
Die Bonding Nozzle			X			+
PCB with SMD				X	+ support	+
Conductive Epoxy	+ contaminate		+ contaminate	+ dispense	X	+ attach
Die	+ Pick and force	+ support		+ support	+ attach	X

Table 3 shows the positive and negative functions including contaminate, dispense, attaché, support, pick and force.

- FA for die bonding process

We transferred Table 2 into Figure 1: function analysis diagram for die bonding process, in which the relationships between components listed in Table 2 were shown in detail.

Fig. 1. Function analysis for die bonding processing

"X": harmful interactions, "⟶": excess interactions, "- - - ->": insufficient interactions.

- All Function Disadvantages

Disadvantages or problems and noted types (harmful, excess, and insufficient) are presented in Table 4.

Table 4. All function disadvantages list

ChK	Function disad. Or problems (Carrier + Action + Object)	Type H/E/I	Target disadv
	Conductive Epoxy contaminates die bonding nozzle	H	Some materials from epoxy attached on die bonding nozzle
	Die collet picks and absorbs/vacuums die	E	Die collets caused a punched hole when it picks the die coarsely
	Conductive Epoxy contaminates die collet	H	Some materials from epoxy attached on die collet
	AU Wire bonding die insufficiently	I	The heating temperature/force isn't sufficient
	AU Wire bonding PCB insufficiently	I	The heating temperature/force isn't sufficient
	Diamond Saw cut molded PCB	E	Sawing molded PCB inaccurately
	Soldering past connect SMD	I	Soldering past melted and connect to SMD poorly

Notes: H: Harmful, E: Excess, I: Insufficient.

- In Figure 2, a CECCA diagram is drawn based on the Cause Effect and Contradiction Chain Analysis in Table 4. CECCA can be used to distinguish and find out the key negative factors in the engineering system. From the target problem, we can, step by step, trace out the negative factors until the target factors of origin are located.

Fig. 2. Cause Effect and Contradiction Chain Analysis Diagram

The target disadvantages and the means to solve the disadvantages are figured out from the analysis in Figure 2.

3.2 Physical and Engineering Contradictions

As we mentioned above, there are contradictions between components. We analyzed them from physical and technical points of view.

- What is the engineering contradiction?

If we use the collet and the nozzle, **then** the chips are successfully picked up. **But** are they vulnerable to particle contamination? (Manufacture)

- What is the physical contradiction?

To have a high performance, **we need to use** collet and nozzle. **But**, **to have endurance** of the system, **we don't want** to use collet and nozzle.

Therefore, we looked into 40 Principles Extend Edition and we found the solutions to solve these problems and contractions.

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Table 5. Solutions suggested by 40 Principles Extended Edition

Worse/ Improve	Performance
Harmful emissions (contamination) Other harmful effects generated by system	35 Parameter changes 24 Intermediary 18 Mechanical Vibration 28Mechanics Substitution 19 Periodic Action 15 Dynamization 4 Asymmetry 33 Homogeneity 3 Local Quality

- What is the engineering contradiction?

If picking up the die is necessary, **then** we need to use a nozzle. **But** it is difficult to do so because the dies will be damaged.

- What is the physical contradiction?

An industrial plastic nozzle is usually more durable.

However, if we want to prevent the dies from damage, it is recommended not to use an industrial plastic nozzle.

Table 6. Solutions suggested by 40 Principles Extended Edition

Worse/ Improve	Performance
Control Complexity Manufacture Precision Productivity Manufacturability Measure Precision	1 Segmentation 2 Taking out/ Separation 3 Local Quality 4 Asymmetry 15 Dynamization 25 Self-Service 28 Mechanics Substitution 35 Parameter Changes 37 hermal Expansion

3.3 Sub-Fields Analyses

Sub-fields is a tool to analyze the relationship between Target and tool. And we found out four ideas 5, 6, 7, and 8 to improve our problems.

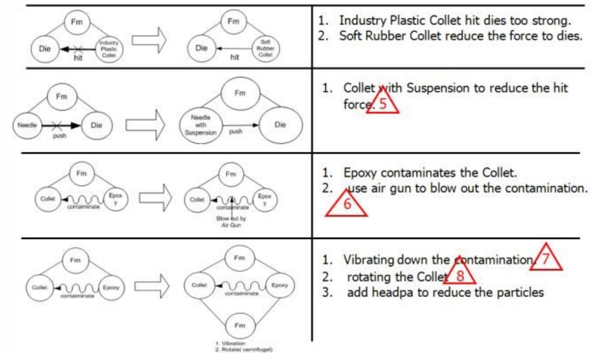
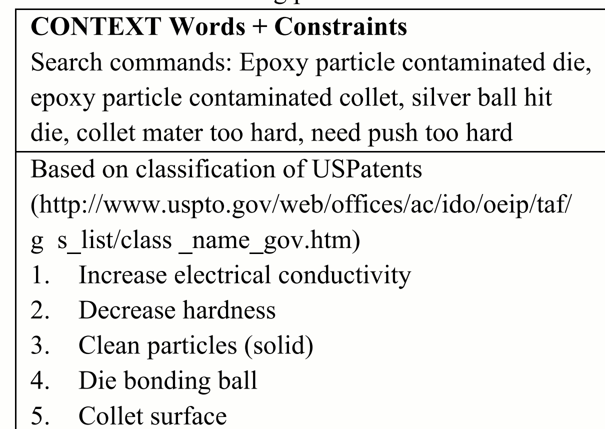


Fig. 3. The analysis using sub-fields to solutions

3.4 Patent and Web Search

Figure 4 is a combination of patent search, in which the whole thinking process is shown.



CONTEXT Words + Constraints
Search commands: Epoxy particle contaminated die, epoxy particle contaminated collet, silver ball hit die, collet mater too hard, need push too hard

Based on classification of USPatents (http://www.uspto.gov/web/offices/ac/ido/oeip/taf/g s_list/class _name_gov.htm)
1. Increase electrical conductivity
2. Decrease hardness
3. Clean particles (solid)
4. Die bonding ball
5. Collet surface

Fig. 4. A structure of patent search

The steps in Figure 4 lead us to the following patent search results in Table 7:

Table 7. Patent search results

#	Source	Patent #	Key Function/Attribute	Key Ideas	attachment
	European Patents	EP1382708 A2	Surface recovery of contaminated deposition tools	Centrifugal fan to detach particle	https://docs.google.com/viewer?url=patentimages.storage.googleapis.com/pdfs/a4c805fcd4caa5e6d1c5/EP1382708A2.pdf
	US Patents	WO 2009003318 A1	Suspension design for high shock performance soldering ball bonding	To reduce hit from silver ball to die	https://www.google.com/patents/WO2009003318A1?cl=en&dq=ball+bonding+design&hl=en&sa=X&ei=j-GyUe7yGsTAkAXByIGoDw&ved=0CDoQ6AEwAA
	US Patents	WO 2008004850 A1	Collet head for placing machine	To find softer collet	https://www.google.com/patents/WO2008004850A1?cl=en&dq=soft+collet+material&hl=en&sa=X&ei=neKyUb-IO8KxkAXy4ICIDg&ved=0CEEQ6AEwAQ

3.5 Function Oriented Search

The key problem which needs to be solved in the die bonding process is that: if we want to achieve an assembling yield over 95%, a conductive epoxy is usually needed to well hold the Chips on to the PCB.

But the conductive epoxy will contaminate the Die Collet and the Bonding Nozzle which causes damage (harm) to the Chips and leads to product failure. The Specific key function of the system is to bond small Chips onto the PCB. But consideration should be given to design specification, diamond saw specification, selecting materials, parameter setting, and contaminations. The required parameter (value ranges) is that Overall Yield must be over 95%. Precision, type of materials, high frequency, materials must be held and joined solidly. The generalized function is Multichip Module IC to be assembled on a single substrate and the overall Yield is expected to be over 95% after final test. A die bonding machine in IC packaging, made by The ID Possible technologies & Leading industry, comes with various types of Collet, some of which are made of steel while others are made of industrial plastic or soft rubber material.

3.6 Search Function Data Base and Patent Data Base

The data bases used in this study for function finding are listed below.
http://www.oxfordcreativity.com
http://function.creax.com/
http://www.triz.co.kr/TRIZ/frame.html
Patent Search web sites
http://patft.uspto.gov/ (USA patents)
http://ep.espacenet.com/ (European patents)
http://www.google.com/patents (free)
http://www.freepatentsonline.com/ (free)
http://www.runride.com/patent/pat_info_all.asp (Taiwan+Japan+China Patents)
http://twp.apipa.org.tw/default.asp (Taiwanese Patents)
http://www.patent.org.tw/
http://www.twpat.com/webpat/
http://www.ipdl.ncipi.go.jp/homepg_e.ipdl (Japanese Patents)

- Original Functions
  (1) Surface recovery of contaminated deposition tools.
  (2) Suspension design for high shock performance die bonding.
  (3) Collet head for placing machine.

- Basic Functions
  (1) Surface recovery of contaminated deposition tools.
  (2) Suspension design for high shock performance die bonding.
  (3) Collet head for placing machine.

- Effects
  (1) To prevent contamination in Collet.
  (2) To reduce hit by Collet with silver ball.
  (3) To change the Collet head with softer surface.

- Specific Approaches
  (1) By using centrifugal fan with specific frequency in order to remove attached particle on Collet.
  (2) A design of specific machine with air compressed pressure to reduce the contact between silver bonding ball and the die.
  (3) Using different axis of design and different material to find the best Collet for semiconductor assembly line.

After summarizing the above discussion, the study comes up with some ideas for improvement.

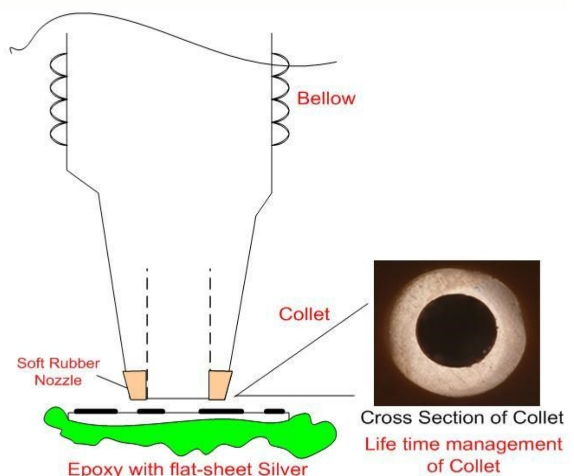


Fig. 5 Ideas to solve the low yield problem

4. Photos Show the Damages on Dies

To check dents, a microscope under 200x and 500x was used and Figure 6 shows that the die was punched.

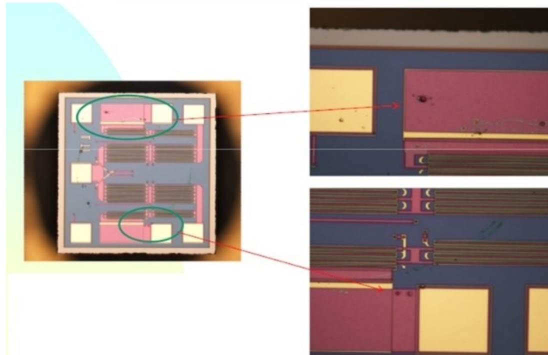


Fig. 6. The die was damaged under microscope

The two photos in Figure 7 are from two different dies. We can see the punched dents occurred in the same place on the surface of both dies. It means the picking nozzle damaged the dies under same nozzle.

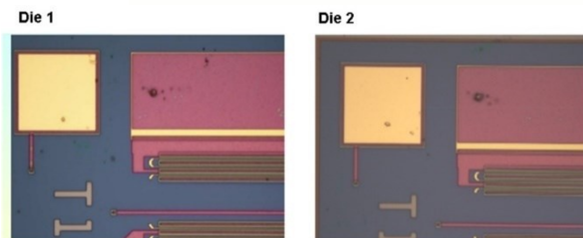


Fig. 7. Two dies were damaged with the same phenomenon in the same place

There are some craters on the tip of nozzle which punches the dies while picking them up.

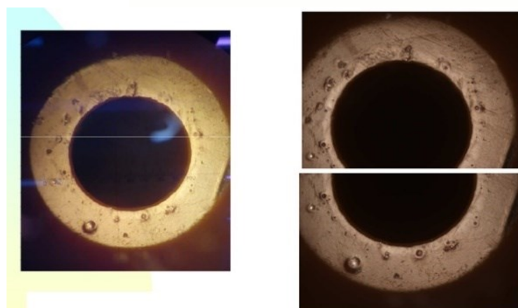


Fig. 8. The tip of Collet (Nozzle) has some craters damaged by silver balls in conductive epoxy.

The photo shows the punched holes completely matched those craters on the nozzle.

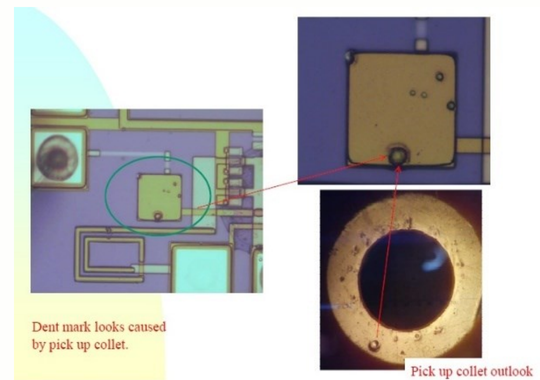


Fig. 9. The dent is matched with the tip of Collet damaged by silver ball.

The photo show that the crater was not punched through. It means it was not damaged by ESD.

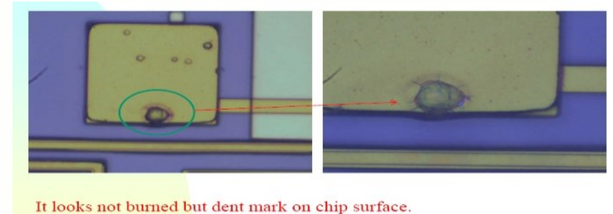


Fig. 10. The dent mark in the chip surface was punched by collet.

The circle on the die (right side) matches the tip of collet.

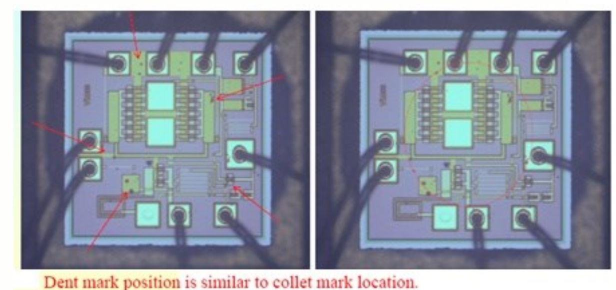


Fig. 11. The circle matches the round-shape of the Collet tip

5. Sip Process Improvement and Actions Taken

In order to improve the assembling process, we need to update SOP to achieve high yield to reduce the cost. Therefore, the lot size is restrained to lower the risks. The standard size was limited to 1000 pcs/ lot.

Table 8, Table9, and Table 10 describe the changes to MCM/SiP assembling process. These changes are designed to prevent the catastrophic failure during the assembling of the SiPs.

- Nozzle and Collet lifetime management (Table 8)
- Nozzle and Collet inspection schedule (Table 9)
- Die visual checking after die bonding (Table 10)

Table 8. Nozzle and Collet lifetime management

Nozzel (Collet) lifetime

Implementation date:	April 22, 2013	
Required Documentation	SOP that describes the lifetime policy of all collects used on the die bond machine.	
Requirement:	Each collect used on the die bond machine has a defined replacement schedule. The lifetime in time or placement are as follows:	
	Collet used on U4 and U5	Time: 6 months Placements: 200,000
	Collet used On U1	Time: 6 months Placement: 200,000
	Collet used on U2	Time: 6 months Placements: 200,000
	Collet used On U3	Time: 6 months Placements: 200,000

Table 9. Nozzle and Collet inspection schedule

Nozzel (Collet) Inspection Schedule

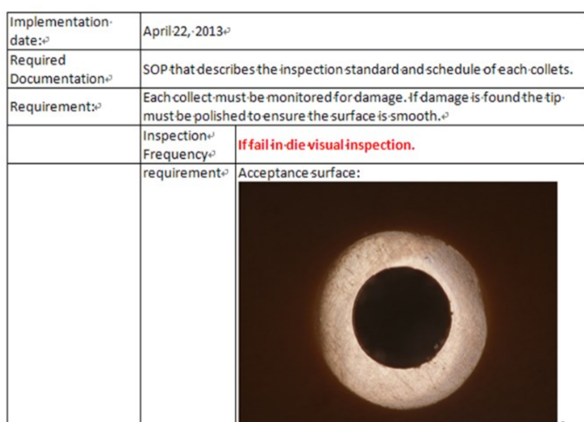
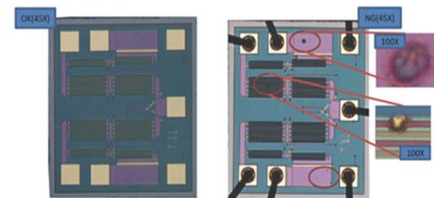
Implementation date:	April 22, 2013	
Required Documentation	SOP that describes the inspection standard and schedule of each collets.	
Requirement:	Each collect must be monitored for damage. If damage is found the tip must be polished to ensure the surface is smooth.	
	Inspection Frequency	If fail in die visual inspection.
	requirement	Acceptance surface: 

Table 10. Die visual checking after die bonding

Die Visual Inspection after Diebond

Implementation Date:	April 22, 2013	
Required Documentation	SOP that describes the inspection standard of each die after it has been bonded.	
Requirement:	after die bonding a sampling of each die is visually inspected for surface damage after being mounted on the PCB.	
	Inspection Frequency	1. Inspect the dies surface at 1st article. Sample size 5 SiPs 2. After 1 st inspection, check it using microscope once per 500 pcs. Sample size 5 Sips.
	Requirement	No any die damaged.

Example Inspection Criteria:



備註：若有晶片外觀NG，利用無塵布清潔collect，再次固晶確認晶片外觀，
若仍有壓痕或異常,請敲機故,通知製程工程部確認

6. Discussion and Conclusion

After we used TRIZ processes, we made great improvement by the following changes:

- Industry Plastic Collet is changed to Soft Rubber Collet.
- Particle control and Collet life checking management are taken.
- Silver-Ball Epoxy is changed to Flat-Sheet conductive epoxy.
- Change thickness of Gold Plating to improve wire bonding.
- Adjust the wire bonding machine's ultrasound power and temperature.
- Change air vent to seal leaking of molding compound.
- Adjust the doping of molding material to change the expansion and extraction characteristics.
- Dicing saw life management.

The contribution and positive impact for the company:

- 15,000 pieces of good products were lost during the Chinese New Year Holiday in 2013 and the total material loss was NTD1.5 million. The delivery schedule to our customers was delayed by two months.
- We solved the MCM problems within 3 days using TRIZ systematic method; otherwise, we would have spent two weeks tracking down the cause of the damage.
- Improve the yield up to 97%.

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Dongliang, Daniel Sheu is a Professor at National Tsing Hua University in Taiwan since 1996. Before then, he has 9 years of industrial experience in the electronic industries with Hewlett-Packard, Motorola, and Matsushita. Daniel received his Ph.D. degree in engineering from UCLA and MBA degree from Kellogg Graduate School of Management at Northwestern University. He also holds a B.S.M.E. degree from National Taiwan University and an M.S.M.E. degree from State University of New York at Buffalo. He is currently the President of the Society of Systematic Innovation and Editor-in-chief of the International Journal of Systematic Innovation. His areas of interests include Systematic Innovation including TRIZ, Design & Manufacturing Management, Equipment Management, and Factory Diagnosis.

Appendix 1: Terminology List

	Term	Full name	Descriptions
1	Curing Oven		molding material baking oven
2	Laser Machine		for laser marking
3	Mold Chase		to shape the IC
4	Epoxy curing Oven		Oven for heating the epoxy
5	Die Colet		A nozzle for picking up dies from wafer
6	Preciser		A plate for aligning the orientation of die
9	Die Nozzle		A nozzle for picking die to bond on PCB
7	Molding Material		Plastic material to cover parts on substrate
10	SMD	Surface Mount Device	Surface mount device
11	Conductive Epoxy		Material gluing the die and PCB
12	Dispenser		A machine spreading glue on PCB
13	Solder Past		A liquid type of Tim to connect the SMD and PCB
14	PCB	Print Circuit Board	Print circuit board
15	Au Wire		Gold wire
16	Diamond Saw		a sawing machine with Diamond cutter
17	SiP	System in package	An integrated multi-chips on a single carry as an IC
18	MCM	Multi-chip Module	An integrated multichip as module but IC outline
5	LTCC	Low temperature co- fired ceramic	Ceramic substrate
6	Molding		The processing of compound material covering on the IC
7	MCU	Main Control Unit	A central unit for a computer system
8	RF	Radio Frequency	Radiated wave which carries signal
9	Transceiver		A part who plays transmitting and receiving
10	yield		The percentage of good and bad rate
11	SMT	Surface Mount Technology	The technology of Soldering the Surface-mount device
12	Curing		After molding, the material was baked for solidating